# COURSE DESCRIPTION CARD - SYLLABUS

Course name
Synchronous Digital Hierarchy (SDH)

## Course

Field of study
Electronics and Telecommunications
Area of study (specialization)

Level of study

Form of study

Year/Semester
II/II
Profile of study

Course offered in
Polish
Requirements

## Number of hours

Lecture
30
Laboratory classes

Other (e.g. online)

Tutorials
0
Projects/seminars
30

## Number of credit points

4

## Lecturers

Responsible for the course/lecturer:
dr hab. inż. Mieczysław Jessa

mieczyslaw.jessa@put.poznan.pl

Responsible for the course/lecturer:

## Prerequisites

Students know the principles, with necessary mathematical background, theory of communication necessary to understand, analyze and evaluate the operation of analogue and digital transmission systems. Is able to extract information from Polish or English language literature, databases and other sources, is able to synthesize gathered information, draw conclusions, and justify opinions.

## Course objective

The presentation of the properties of the basic transmission system that is used to send information between nodes of contemporary communication networks. This system is known as Synchronous Digital Hierarchy (SDH). To create skills necessary to design multiring SDH networks.

## Course-related learning outcomes

### Knowledge

1. Has an advanced knowledge about construction and operation of communication systems used in multimedia transmission.

### Skills

1. Is able to design, analyze, construct and maintain technically advanced communication systems, including various devices and networks being elements of such systems. Is able to ensure required technical parameters of the designed systems.

2. Is able to select adequate methods to solve typical tasks related to analysis, design and optimization of transmission systems.

### Social competences

1. Is responsible for the designed electronic and communication systems and knows physical and social threats that can appear as the result of irresponsible design or usage of communication systems.

2. Is aware of the necessity to approach solving technical problems with responsibility and professionalism.

## Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Learning outcomes are verified with a written/oral test. Test consists of 5 open questions. Answers are scored equally. Minimum number of scores to pass the exam is equal to 50%. The set of predefined subjects is sent to students by email.

Knowledge and skills gathered during the Project are assessed by written project and oral presentation of the results of this project. The final mark is the average of two marks. The assessment levels are the following: under 3 - mark 2.0, from 3 to 3.25 - mark 3.0; from 3.26 to 3.75 - mark 3.5; from 3.76 to 4.25 - mark 4.0; from 4.26 to 4.75 - mark 4.5; above 4.75 - mark 5.0.

## Programme content

During the course students learn about advanced properties of SDH and NG-SDH hierarchies and about mathematical modelling of transmission systems. Program content includes: genesis of SDH, the layer and line model of SDH, the concept of container and virtual container, tributary unit, tributary unit group, pointer, pointer justifications, administrative unit,

synchronous transport module level n, where n can be equal to 0, 1, 4, 16, 64, 256, methods of mapping bit streams into SDH containers, the concept of tandem connection, methods of protection and alarm signals, types of SDH multiplexers, SDH clocks and methods of their synchronization, the concept of functional, physical and information architecture of SDH, general models of protection, vertical and horizontal partition of a network and a network connection, topologies of SDH networks (linear, ring, mesh), protection methods offered by SDH rings, methods of interconnection of rings, methods of building hierarchical SDH network composed of many rings, methods of designing multiring SDH networks, examples of SDH networks in various countries. Students learn about NG-SDH, virtual concatenation V-CAT, Link Capacity Adjustment Scheme (LCAS), and Generic Framing Procedure (GFC) used in NG-SDH.

The goal of the Project is to prepare and implement in FPGA or SoC a chosen component of the SDH system or to design a multiring SDH network for given bit rates between neighbor nodes. Student can choose a component type or input data from prepared by the teacher or can propose his own subject, after earlier acceptance of the teacher. Among existing propositions we have: SDH multiplexer that multiplexes four STM-1 signals into one STM-4 signal; synchronization circuit for SDH multiplexer, synchronized with 2048 kb/s signal; a circuit/software for BER assessment in RSOH or MSOH or VC-4, or VC-12; phase detector for wander and jitter measurements, a circuit that can assess the power of STM-1 signal at the input of SDH multiplexer; sinusoidal jitter generator with known parameters; computer model of multiplexing four AU-4 into AU-4-4; computer model of asynchronous mapping of E1 signals into C-12 container; computer model of error detection with BIP-K, where K can assume 2, 8 or 16; header generator and visualizer for STM-1 frame.

## Teaching methods

Lecture: Multimedia presentation.

Project: A combination of exercise and project method.

## Bibliography

Basic

1. R. K. Jain „Principles of Synchronous Digital Hierarchy”, CRC Press, Boca Raton, 2013.

2. Sławomir Kula „Systemy Teletransmisyjne”, WKŁ, Warszawa, 2004

Additional

1. A. Valdar „Understanding Telecommunications Networks”, IET, London, 2006.

2. B.G. Lee, M. Kang, J. Lee „Broadband Telecommunications Technology”, Artech House, 2nd. Edn. Boston, 1996.

3. M. Sexton, A. Reid ”Broadband Networking, ATM, SDH, and SONET”, Artech House, Boston, 1997

## Breakdown of average student's workload

| | Hours | ECTS |
|---|---|---|
| Total workload | 100 | 4,0 |
| Classes requiring direct contact with the teacher | 70 | 3,0 |
| Student's own work (literature studies, preparation for laboratory classes/tutorials, preparation for tests/exam, project preparation) [1] | 30 | 1,0 |

[1] delete or add other activities as appropriate